1. An integrated circuit comprising:

a first device comprising a first lead, a second lead, and a third lead, wherein said third lead of said first device is electrically connected to ground; and

a second device comprising a first lead, a second lead, and a third lead, wherein said third lead of said second device is electrically connected to ground;

wherein the effective threshold voltage of said first device is more susceptible to be lowered by ionizing radiation than is the effective threshold voltage of said second device.

2. The integrated circuit of claim 1 wherein said first device comprises an *n*-type metal-oxide semiconductor field-effect transistor.

3. The integrated circuit of claim 1 wherein said first device comprises a field oxide that has been implanted with a material that traps positive charge when said first device is exposed to ionizing radiation and said second device has not been implanted with said material.

4. The integrated circuit of claim 1 wherein said integrated circuit further comprises a microprocessor that comprises a control sequencer coupled to an arithmetic logic unit.

5. The integrated circuit of claim 1 wherein said integrated circuit further comprises an arrangement of memory cells operatively coupled to an address decoder.

6. The integrated circuit of claim 1 wherein said second lead of said first device is connected to ground, said third lead of said first device is connected to power, and said third lead of said second device is connected to power.

7. The integrated circuit of claim 1 wherein said first device shorts power to ground when said device has been exposed to ionizing radiation.

8. An integrated circuit comprising:

a first device comprising a first lead, a second lead, and a third lead, wherein said third lead of said first device is electrically connected to ground; and

a second device comprising a first lead, a second lead, and a third lead, wherein said third lead of said second device is electrically connected to ground;

wherein at least a portion of said first device comprises a higher concentration of positive charge trapping centers than said second device.

9. The integrated circuit of claim 1 wherein said first device comprises an *n*-type metal-oxide semiconductor field-effect transistor.

10. The integrated circuit of claim 1 wherein said integrated circuit comprises a microprocessor that comprises a control sequencer and arithmetic logic unit.

11. A method comprising:

fabricating a base layer comprising a first device having a first lead and a second lead, and a second device having a first lead that is electrically connected to said first lead of said first device;

implanting at least a portion of said first device with a material that traps positive charge when said first device is exposed to ionizing radiation; and

preventing said second device from being implanted with said material.

12. The method of claim 11 wherein said first device comprises an *n*-type metal-oxide semiconductor field-effect transistor.

13. The method of claim 11 wherein a field oxide in an isolation region associated with said first device is implanted with said material.

14. The method of claim 11 further comprising masking said base layer with a resist to protect said second device from being implanted with said material and to expose said first device to being implanted with said material.

15. A method comprising:

fabricating a base layer comprising a first device having a first lead and a second lead, and a second device having a first lead that is electrically connected to said first lead of said first device;

masking said base layer with a resist to protect said second device from an implantation that traps positive charge when said second device is exposed to ionizing radiation, and to expose said first device to said implantation; and

implanting at least a portion of said first device with said implantation.

16. The method of claim 15 wherein said first device comprises an *n*-type metal-oxide semiconductor field-effect transistor.

17. The method of claim 15 wherein a field oxide in an isolation region associated with said first device is implanted with said material.

18. A method of operating an integrated circuit, said method comprising:

processing signals with a first device; and

interfering with the operation of said first device with a second device when and only when said integrated circuit is exposed to ionizing radiation.

19. The method of claim 18 wherein the exposure of said integrated circuit to ionizing radiation shorts an output of said first device to ground through said second device.

20. The method of claim 18 wherein at least a portion of said second device comprises an implant that facilitates the trapping of positive charge when exposed to ionizing radiation that said first device does not comprise.

21. The method of claim 18 wherein the exposure of said integrated circuit to ionizing radiation disables the operation of said integrated circuit.